

# 1991 Index

## IEEE Transactions on Semiconductor Manufacturing

### Vol. 4

This index covers all items — papers, correspondence, reviews, etc. — appeared in this periodical during 1991, and items from previous years were commented upon or corrected in 1991.

The *Author Index* contains the primary entry for each item, listed under first author's name, and cross-references from all coauthors. The *Subject Index* contains several entries for each item under appropriate subject headings, and subject cross-references.

It is always necessary to refer to the primary entry in the *Author Index* for exact title, coauthors, and comments/corrections.

#### AUTHOR INDEX

##### A

- gino, Alice M., *see* Nadi, Fariborz, *T-SEM Feb 91* 52-58  
 , K.-H., *see* Campbell, Stephen A., *T-SEM Feb 91* 14-20  
 yama, Shigenobu, *see* Uraoka, Yukiharu, *T-SEM Aug 91* 183-192  
 n, Susan L., *see* Friedman, David J., *T-SEM Feb 91* 36-42  
 uita, José, *see* Cané, Carles, *T-SEM Aug 91* 199-205

##### B

- nan, Bruce A., and Akira Ito. Generation of electromigration ground rules utilizing Monte Carlo simulation methods (Corresp.); *T-SEM Feb 91* 63-66  
 gadde, L. G., *see* Choudhury, Debabani, *T-SEM Feb 91* 69-72  
 Michael, Marc Rocchi, and Jan Engel. Realistic statistical worst-case simulations of VLSI circuits; *T-SEM Aug 91* 193-198  
 er, Alison, *see* Gernal, Robert, *T-SEM Nov 91* 298-303  
 ges, Andrew D., *see* Lendenmann, Heinz, *T-SEM Aug 91* 213-218  
 ley, Steven K., *see* Kazior, Thomas E., *T-SEM Feb 91* 21-25  
 h-Vishniac, Ilene, *see* Wang, Ing-Yann Albert, *T-SEM May 91* 145-154

##### C

- uja, Enric, *see* Cané, Carles, *T-SEM Aug 91* 199-205  
 obell, Stephen A., K.-H. Ahn, Karson L. Knutson, Benjamin Y. H. Liu, and John D. Leighton. Steady-state thermal uniformity and gas flow patterns in a rapid thermal processing chamber; *T-SEM Feb 91* 14-20  
 , Carles, Manuel Lozano, Enric Cabruja, José Anguita, Emilio Lora-Tamayo, and Francisco Serra-Mestres. Latch-up characterization using novel test structures and instruments; *T-SEM Aug 91* 199-205  
 g, Edward Y., Richard Dean, James Proctor, Robert Elmer, and Krishna Pande. A hybrid wafer-dicing process for GaAs MMIC production (Corresp.); *T-SEM Feb 91* 66-68  
 g, Norman H., and Costas J. Spanos. Continuous equipment diagnosis using evidence integration: An LPCVD application; *T-SEM Feb 91* 43-51  
 dhury, Debabani, L. G. Bhatgadde, and S. Mahapatra. Selective electrolessplating—A new technique for GaAs MMIC's (Corresp.); *T-SEM Feb 91* 69-72  
 au, Alain R., and Normand Nadeau. Modeling the bending of probes used in semiconductor industry; *T-SEM May 91* 122-127

##### D

- Richard, *see* Chang, Edward Y., *T-SEM Feb 91* 66-68  
 amo, Jesús A., *see* Moran, Peter W., *T-SEM Nov 91* 304-311

##### E

- , Scott, *see* Moran, Peter W., *T-SEM Nov 91* 304-311  
 , Robert, *see* Chang, Edward Y., *T-SEM Feb 91* 66-68  
 Jan, *see* Bolt, Michael, *T-SEM Aug 91* 193-198

##### F

- , Martin, *see* Walton, Anthony J., *T-SEM Aug 91* 233-240  
 nan, David J., and Susan L. Albin. Clustered defects in IC fabrication: Impact on process control charts; *T-SEM Feb 91* 36-42

##### G

- Gammie, William, *see* Walton, Anthony J., *T-SEM Aug 91* 233-240  
 Glang, Reinhard. Defect size distribution in VLSI chips; *T-SEM Nov 91* 265-269  
 Glassey, C. Roger, and W. Willie Weng. Dynamic batching heuristic for simultaneous processing; *T-SEM May 91* 77-82  
 Goto, Haruhiro H., Makoto Sasaki, Tadahiro Ohmi, Tadashi Shibata, Atsushi Yamagami, Nobuyuki Okamura, and Osamu Kamiya. A low damage, low contaminant plasma processing system utilizing energy clean technology; *T-SEM May 91* 111-121  
 Gernal, Robert, Alison Bonner, and Farhang Shadman. Effect of component interactions on the removal of organic impurities; *T-SEM Nov 91* 298-303  
 Grider, Douglas T., *see* Öztürk, Mehmet C., *T-SEM May 91* 155-165  
 Guo, Ruey-Shan, *see* Sachs, Emanuel, *T-SEM May 91* 134-144  
 Gyuresik, Ronald S., Terrence J. Riley, and F. Yates Sorrell. A model for rapid thermal processing: Achieving uniformity through lamp control; *T-SEM Feb 91* 9-13

##### H

- Ha, Sungdo, *see* Sachs, Emanuel, *T-SEM May 91* 134-144  
 Henderson, Rebecca M., *see* Moran, Peter W., *T-SEM Nov 91* 304-311  
 Hirasawa, Shigeki, *see* Watanabe, Tomoji, *T-SEM Feb 91* 59-63  
 Hodges, David A., *see* Nadi, Fariborz, *T-SEM Feb 91* 52-58  
 Holwill, Robert J., *see* Walton, Anthony J., *T-SEM Aug 91* 233-240  
 Holwill, Robert J., *see* Wilson, David, *T-SEM Aug 91* 241-249  
 Hu, Albert, *see* Sachs, Emanuel, *T-SEM May 91* 134-144  
 Huang, Jiahua, *see* May, Gary S., *T-SEM May 91* 83-98

##### I

- Ito, Akira, *see* Beitman, Bruce A., *T-SEM Feb 91* 63-66

##### J

- Johnson, F. Scott, *see* Öztürk, Mehmet C., *T-SEM May 91* 155-165  
 Jones, Robert E., and Thomas C. Mele. Use of screening and response-surface experimental designs for development of a 0.5- $\mu$ m CMOS self-aligned titanium silicide process; *T-SEM Nov 91* 281-287  
 Joosten, Johannes J. M., *see* Swaving, Sieger, *T-SEM Aug 91* 174-182  
 Joosten, Johannes J. M., *see* van der Klauw, Cornelis L. M., *T-SEM Aug 91* 206-212

##### K

- Kamiya, Osamu, *see* Goto, Haruhiro H., *T-SEM May 91* 111-121  
 Kawanabe, Ichiro, *see* Kikyama, Hirohisa, *T-SEM Feb 91* 26-35  
 Kazior, Thomas E., Steven K. Brierley, and Frank J. Piekariski. Capless rapid thermal annealing of GaAs using a graphite susceptor; *T-SEM Feb 91* 21-25  
 Kibarian, John K., and Andrzej Strojwas. Using spatial information to analyze correlations between test structure data; *T-SEM Aug 91* 219-225  
 Kikyama, Hirohisa, Nobuhiro Miki, Kiyonori Saka, Jun Takano, Ichiro Kawanabe, Masayuki Miyashita, and Tadahiro Ohmi. Principles of wet chemical processing in ULSI microfabrication; *T-SEM Feb 91* 26-35  
 Knutson, Karson L., *see* Campbell, Stephen A., *T-SEM Feb 91* 14-20

##### L

- Lee, Chung-Yee, *see* Uzsoy, Reha, *T-SEM Nov 91* 270-280  
 Leighton, John D., *see* Campbell, Stephen A., *T-SEM Feb 91* 14-20  
 Lendenmann, Heinz, Ronald D. Schrimpf, and Andrew D. Bridges. Novel test structure for the measurement of electrostatic discharge pulses; *T-SEM Aug 91* 213-218  
 Leonard, Paul A., *see* Uzsoy, Reha, *T-SEM Nov 91* 270-280  
 Li, Shih-Hung, *see* Wang, Ing-Yann Albert, *T-SEM May 91* 145-154  
 Liu, Benjamin Y. H., *see* Campbell, Stephen A., *T-SEM Feb 91* 14-20  
 Long, Christopher W., *see* Voldman, Steven H., *T-SEM Aug 91* 226-232  
 Lora-Tamayo, Emilio, *see* Cané, Carles, *T-SEM Aug 91* 199-205  
 Lozano, Manuel, *see* Cané, Carles, *T-SEM Aug 91* 199-205



## M

- Mahapatra, S., *see* Choudhury, Debabani, *T-SEM Feb 91* 69-72  
 Manos, Pete, and H. A. Stevens. Effects of backend processing on counter-doped  $N^+$  poly-Si resistance; *T-SEM Nov 91* 288-293  
 Martin-Vega, Louis A., *see* Uzsoy, Reha, *T-SEM Nov 91* 270-280  
 May, Gary S., Jiahua Huang, and Costas J. Spanos. Statistical experimental design in plasma etch modeling; *T-SEM May 91* 83-98  
 Mele, Thomas C., *see* Jones, Robert E., *T-SEM Nov 91* 281-287  
 Miki, Nobuhiro, *see* Kikyuama, Hirohisa, *T-SEM Feb 91* 26-35  
 Miyashita, Masayuki, *see* Kikyuama, Hirohisa, *T-SEM Feb 91* 26-35  
 Moran, Peter W., Scott Elliott, Neil Wylie, Rebecca M. Henderson, and Jesús A. del Alamo. A process control methodology applied to manufacturing GaAs MMIC's; *T-SEM Nov 91* 304-311

## N

- Nadeau, Normand, *see* Comeau, Alain R., *T-SEM May 91* 122-127  
 Nadi, Fariborz, Alice M. Agogino, and David A. Hodges. Use of influence diagrams and neural networks in modeling semiconductor manufacturing processes; *T-SEM Feb 91* 52-58  
 Nakata, Yoshiro, *see* Uraoka, Yukiharu, *T-SEM Aug 91* 183-192

## O

- Ohmi, Tadahiro, *see* Kikyuama, Hirohisa, *T-SEM Feb 91* 26-35  
 Ohmi, Tadahiro, *see* Goto, Haruhiro H., *T-SEM May 91* 111-121  
 Okamura, Nobuyuki, *see* Goto, Haruhiro H., *T-SEM May 91* 111-121  
 Oldham, William G., *see* Partlo, William N., *T-SEM May 91* 128-133  
 Öztürk, Mehmet C., F. Yates Sorrell, Jimmie J. Wortman, F. Scott Johnson, and Douglas T. Grider. Manufacturability issues in rapid thermal chemical vapor deposition; *T-SEM May 91* 155-165

## P

- Pande, Krishna, *see* Chang, Edward Y., *T-SEM Feb 91* 66-68  
 Partlo, William N., and William G. Oldham. Transmission measurements of pellicles for deep-UV lithography; *T-SEM May 91* 128-133  
 Piekarski, Frank J., *see* Kazior, Thomas E., *T-SEM Feb 91* 21-25  
 Proctor, James, *see* Chang, Edward Y., *T-SEM Feb 91* 66-68

## R

- Riley, Terrence J., *see* Gyurcsik, Ronald S., *T-SEM Feb 91* 9-13  
 Robertson, John M., *see* Wilson, David, *T-SEM Aug 91* 241-249  
 Robertson, John M., *see* Walls, Jim A., *T-SEM Aug 91* 250-262  
 Rocchi, Marc, *see* Bolt, Michael, *T-SEM Aug 91* 193-198

## S

- Sachs, Emanuel, Ruey-Shan Guo, Sungdo Ha, and Albert Hu. Process control system for VLSI fabrication; *T-SEM May 91* 134-144  
 Saka, Kiyonori, *see* Kikyuama, Hirohisa, *T-SEM Feb 91* 26-35  
 Sasaki, Makoto, *see* Goto, Haruhiro H., *T-SEM May 91* 111-121  
 Schrimpf, Ronald D., *see* Lendenmann, Heinz, *T-SEM Aug 91* 213-218  
 Serra-Mestres, Francisco, *see* Cané, Carles, *T-SEM Aug 91* 199-205  
 Shadman, Farhang, *see* Govenal, Robert, *T-SEM Nov 91* 298-303  
 Shenai, Krishna. Manufacturability issues related to transient thermal annealing of titanium silicide films in a rapid thermal processor; *T-SEM Feb 91* 1-8  
 Shibata, Tadashi, *see* Goto, Haruhiro H., *T-SEM May 91* 111-121  
 Sorrell, F. Yates, *see* Gyurcsik, Ronald S., *T-SEM Feb 91* 9-13  
 Sorrell, F. Yates, *see* Öztürk, Mehmet C., *T-SEM May 91* 155-165  
 Spanos, Costas J., *see* Chang, Norman H., *T-SEM Feb 91* 43-51  
 Spanos, Costas J., *see* May, Gary S., *T-SEM May 91* 83-98  
 Stapper, C. H. On Murphy's yield integral; *T-SEM Nov 91* 294-297  
 Stevens, H. A., *see* Manos, Pete, *T-SEM Nov 91* 288-293  
 Stevenson, J. T. M., *see* Walton, Anthony J., *T-SEM Aug 91* 233-240  
 Strojwas, Andrzej J., *see* Yuan, Chi-Min, *T-SEM May 91* 99-110  
 Strojwas, Andrzej J., *see* Kibarian, John K., *T-SEM Aug 91* 219-225  
 Swaving, Sieger, Cornelis L. M. van der Klauw, and Johannes J. M. Joosten. Analysis of the determination of the dimensional offset of conducting layers and MOS transistors; *T-SEM Aug 91* 174-182

## T

- Takagaki, Tetsuya, *see* Watanabe, Tomoji, *T-SEM Feb 91* 59-63  
 Takano, Jun, *see* Kikyuama, Hirohisa, *T-SEM Feb 91* 26-35  
 Torii, Takuji, *see* Watanabe, Tomoji, *T-SEM Feb 91* 59-63  
 Tsutsu, Noriko, *see* Uraoka, Yukiharu, *T-SEM Aug 91* 183-192

## U

- Uraoka, Yukiharu, Noriko Tsutsu, Yoshiro Nakata, and Shigeru Akiyama. Evaluation technology of VLSI reliability using hot cathode luminescence; *T-SEM Aug 91* 183-192  
 Uzsoy, Reha, Louis A. Martin-Vega, Chung-Yee Lee, and Paul A. Leonard. Production scheduling algorithms for a semiconductor test facility; *T-SEM Nov 91* 270-280

## V

- van der Klauw, Cornelis L. M., *see* Swaving, Sieger, *T-SEM Aug 91* 174-182  
 van der Klauw, Cornelis L. M., and Johannes J. M. Joosten. Multiplexing force-sense test structures for (MOS) IC applications; *T-SEM Aug 91* 206-212  
 Voldman, Steven H., and Christopher W. Long. TLM: A trenchless monitor for a four megabit SPT DRAM technology; *T-SEM Aug 91* 226-232

## W

- Walls, Jim A., Anthony J. Walton, and J. M. Robertson. Interpretation and control of C-V measurements using pattern recognition and expert system techniques; *T-SEM Aug 91* 250-262  
 Walton, Anthony J., William Gammie, Martin Fallon, J. T. M. Stevenson, and Robert J. Holwill. An interconnect scheme for reducing the number of contact pads on process control chips; *T-SEM Aug 91* 233-240  
 Walton, Anthony J., *see* Wilson, David, *T-SEM Aug 91* 241-249  
 Walton, Anthony J., *see* Walls, Jim A., *T-SEM Aug 91* 250-262  
 Walton, Anthony J., Guest Ed. Introduction to special issue on design of microelectronic test structures for characterization and control of the IC manufacturing process; *T-SEM Aug 91* 173  
 Wang, Ing-Yann Albert, Shih-Hung Li, and Ilene Busch-Vishniac. Magnetic levitation transport path; *T-SEM May 91* 145-154  
 Watanabe, Tomoji, Takuji Torii, Shigeki Hirasawa, and Tetsuya Takagaki. Radiation thermometry of silicon wafers in a diffusion furnace; *T-SEM Feb 91* 59-63  
 Weng, W. Willie, *see* Glassey, C. Roger, *T-SEM May 91* 77-82  
 Wilson, David, Anthony J. Walton, John M. Robertson, and Robert J. Holwill. Characterization of parasitic transistors to evaluate CMOS process uniformity; *T-SEM Aug 91* 241-249  
 Wortman, Jimmie J., *see* Öztürk, Mehmet C., *T-SEM May 91* 155-165  
 Wylie, Neil, *see* Moran, Peter W., *T-SEM Nov 91* 304-311

## Y

- Yamagami, Atsushi, *see* Goto, Haruhiro H., *T-SEM May 91* 111-121  
 Yuan, Chi-Min, and Andrzej J. Strojwas. Modeling optical equipment for wafer alignment and line-width measurement; *T-SEM May 91* 99-110

## SUBJECT INDEX

## A

- Air insulation; *cf.* Electrostatic discharges  
 Annealing; *cf.* Process heating

## B

- Bending; *cf.* Contacts, mechanical factors  
 Bipolar-CMOS integrated circuits  
 characterization of parasitic bipolar and MOS transistors to evaluate CMOS process uniformity. *Wilson, David, + , T-SEM Aug 91* 241-249

## C

- CAM (computer-aided manufacturing); *cf.* Manufacturing automation  
 Capacitance measurement  
 interpretation and control of C-V measurements using pattern recognition and expert system techniques; C-V EXPERT. *Walls, Jim A., + , T-SEM Aug 91* 250-262  
 Carbon materials/devices  
 removing organic impurities in ultrapure water systems; effect of component interactions with UV radiation. *Govenal, Robert, + , T-SEM Nov 91* 298-303  
 statistical experimental design in  $CCl_4$ -plasma-etch modeling. *May, Gary S., + , T-SEM May 91* 83-98



carbon materials/devices; cf. Graphite  
 large-carrier processes  
 evaluating VLSI reliability using hot carrier luminescence. *Uraoka, Yukiharu*, +, *T-SEM Aug 91* 183-192  
 circuit reliability; cf. Integrated-circuit reliability  
 clustering methods; cf. Pattern clustering methods  
**CMOS integrated circuits**  
 characterization of parasitic bipolar and MOS transistors to evaluate CMOS process uniformity. *Wilson, David*, +, *T-SEM Aug 91* 241-249  
 effects of backend processing on counterdoped N<sup>+</sup> poly-Si resistance. *Manos, Pete*, +, *T-SEM Nov 91* 288-293  
 latch-up characterization using novel test structures and instruments for CMOS processes. *Cané, Carles*, +, *T-SEM Aug 91* 199-205  
 self-multiplexing force-sense test structures for MOS IC applications. *van der Klauw, Cornelis L. M.*, +, *T-SEM Aug 91* 206-212  
 using screening and response-surface experimental designs to develop 0.5- $\mu$ m CMOS self-aligned titanium silicide process. *Jones, Robert E.*, +, *T-SEM Nov 91* 281-287  
**CMOS integrated circuits, memory**  
 trench current leakage monitor for 4-Mb SPT CMOS DRAM technology. *Voldman, Steven H.*, +, *T-SEM Aug 91* 226-232  
**CMOSFET circuits; cf. CMOS integrated circuits**  
**CMOSFET switches**  
 trench current leakage monitor for 4-Mb SPT CMOS DRAM technology. *Voldman, Steven H.*, +, *T-SEM Aug 91* 226-232  
**CMOSFETs; cf. CMOS integrated circuits**  
 component reliability; cf. Integrated-circuit reliability  
 computer-aided manufacturing; cf. Manufacturing automation  
 defects; cf. Integrated-circuit metallization  
 defects, mechanical factors  
 modeling the bending of probes used in semiconductor industry. *Comeau, Alain R.*, +, *T-SEM May 91* 122-127  
 control systems; cf. Manufacturing automation; Process control  
 correlation  
 using spatial information to analyze correlations between chip test structure data. *Kibarian, John K.*, +, *T-SEM Aug 91* 219-225  
 trench measurement  
 trench current leakage monitor for 4-Mb SPT CMOS DRAM technology. *Voldman, Steven H.*, +, *T-SEM Aug 91* 226-232  
 processing; cf. Materials processing

## D

diagnosis; cf. Fault diagnosis  
 dielectric breakdown; cf. Electrostatic discharges  
 dielectric measurements; cf. Capacitance measurement  
 digital integrated circuits; cf. CMOS integrated circuits; Large-scale integration; MOS integrated circuits; Very-large-scale integration  
 distribution functions; cf. Probability

## E

electric variables measurement; cf. Capacitance measurement; Current measurement; Integrated-circuit measurements; Voltage measurement  
 modes  
 modeling the bending of probes used in semiconductor industry. *Comeau, Alain R.*, +, *T-SEM May 91* 122-127  
 electromigration; cf. Integrated-circuit metallization  
 electrostatic discharges  
 chip test structure for the measurement of electrostatic discharge pulses. *Lendenmann, Heinz*, +, *T-SEM Aug 91* 213-218  
 electrostatic interference; cf. Electrostatic discharges  
 etching; cf. Electrostatic discharges  
 etching; cf. Plasma applications, materials processing  
 fault systems  
 continuous semiconductor manufacturing equipment diagnosis using evidence integration; LPCVD application. *Chang, Norman H.*, +, *T-SEM Feb 91* 43-51  
 interpretation and control of C-V measurements using pattern recognition and expert system techniques; C-V EXPERT. *Walls, Jim A.*, +, *T-SEM Aug 91* 250-262

## F

fabrication; cf. Integrated-circuit fabrication; Materials processing; Semiconductor device fabrication; Thin-film circuit fabrication  
 factory automation; cf. Manufacturing automation  
 failure analysis; cf. Fault diagnosis  
 fault diagnosis  
 continuous semiconductor manufacturing equipment diagnosis using evidence integration; LPCVD application. *Chang, Norman H.*, +, *T-SEM Feb 91* 43-51

FET integrated circuits; cf. CMOS integrated circuits; MOS integrated circuits  
**FET integrated circuits, memory; cf. CMOS integrated circuits, memory**  
**FET switches; cf. CMOSFET switches**  
**FETs; cf. JFETs; MOSFETs**  
**Fluid flow control**  
 steady-state thermal uniformity and gas flow patterns in rapid thermal processing chamber; numerical calculations for various process conditions. *Campbell, Stephen A.*, +, *T-SEM Feb 91* 14-20  
**Force measurement**  
 self-multiplexing force-sense test structures for MOS IC applications. *van der Klauw, Cornelis L. M.*, +, *T-SEM Aug 91* 206-212  
**Forecasting**  
 dynamic batching heuristic for simultaneous processing; using event forecasting to reduce wait time in CIM environment. *Glassey, C. Roger*, +, *T-SEM May 91* 77-82

## G

**Gallium materials/devices**

capless rapid thermal annealing of GaAs using graphite susceptor. *Kazior, Thomas E.*, +, *T-SEM Feb 91* 21-25  
 hybrid wafer-dicing process for GaAs MMIC production using spin-on wax. *Chang, Edward Y.*, +, *T-SEM Feb 91* 66-68  
 methodology for guiding process-driven manufacturing organizations in instituting process control on facilitywide basis. *Moran, Peter W.*, +, *T-SEM Nov 91* 304-311  
 selective electroless plating for GaAs MMIC transmission line fabrication. *Choudhury, Debabani*, +, *T-SEM Feb 91* 69-72

**Gas flow control; cf. Fluid flow control****Gradient methods**

realistic statistical worst-case simulations of VLSI circuits using gradient analysis. *Bolt, Michael*, +, *T-SEM Aug 91* 193-198

**Graphite**

capless rapid thermal annealing of GaAs using graphite susceptor. *Kazior, Thomas E.*, +, *T-SEM Feb 91* 21-25

## H

**Heating; cf. Process heating****Hybrid integrated-circuit fabrication; cf. Thin-film circuit fabrication****Hydrogen materials/devices**

principles of wet chemical processing in ULSI microfabrication using advanced surface-active buffered hydrogen fluoride. *Kikyuama, Hirohisa*, +, *T-SEM Feb 91* 26-35

## I

**Identification; cf. Pattern recognition****Image classification; cf. Pattern recognition****Industrial control; cf. Manufacturing automation; Process control****Integral equations**

exact solution to Murphy's yield integral for compounding statistical distributions. *Stapper, C. H.*, *T-SEM Nov 91* 294-297

**Integrated-circuit bonding; cf. Integrated-circuit interconnections****Integrated-circuit design; cf. Yield optimization****Integrated-circuit doping; cf. Integrated-circuit ion implantation****Integrated-circuit fabrication**

clustered defects in IC fabrication; impact on process control charts. *Friedman, David J.*, +, *T-SEM Feb 91* 36-42  
 continuous semiconductor manufacturing equipment diagnosis using evidence integration; LPCVD application. *Chang, Norman H.*, +, *T-SEM Feb 91* 43-51  
 design and use of microelectric test structures for characterization and control of IC manufacturing process (special issue). *T-SEM Aug 91* 173-262  
 manufacturability issues in rapid thermal chemical vapor deposition. *Öztürk, Mehmet C.*, +, *T-SEM May 91* 155-165  
 principles of wet chemical processing in ULSI microfabrication using advanced surface-active buffered hydrogen fluoride. *Kikyuama, Hirohisa*, +, *T-SEM Feb 91* 26-35  
 transmission measurements of pellicles for deep-UV lithography. *Partlo, William N.*, +, *T-SEM May 91* 128-133  
 using screening and response-surface experimental designs to develop 0.5- $\mu$ m CMOS self-aligned titanium silicide process. *Jones, Robert E.*, +, *T-SEM Nov 91* 281-287



**Integrated-circuit fabrication; cf.** Integrated-circuit ion implantation; Integrated-circuit metallization; Large-scale integration; Manufacturing automation; Materials processing; Plasma applications, materials processing; Process heating; Thin-film circuit fabrication; Ultra-large-scale integration; Very-large-scale integration

#### Integrated-circuit interconnections

defect size distribution in VLSI chips; analytical model for short circuits related to line spacing. *Glang, Reinhard, T-SEM Nov 91 265-269*  
multiplexed interconnect scheme for reducing number of contact pads on process control chips. *Walton, Anthony J., +, T-SEM Aug 91 233-240*

#### Integrated-circuit ion implantation

effects of backend processing on counterdoped  $N^+$  poly-Si resistance. *Manos, Pete, +, T-SEM Nov 91 288-293*

**Integrated-circuit ion implantation; cf.** Plasma applications, materials processing

#### Integrated-circuit measurements

chip test structure for the measurement of electrostatic discharge pulses. *Lendenmann, Heinz, +, T-SEM Aug 91 213-218*

modeling optical equipment for wafer alignment and line-width measurement. *Yuan, Chi-Min, +, T-SEM May 91 99-110*

modeling the bending of probes used in semiconductor industry. *Comeau, Alain R., +, T-SEM May 91 122-127*

trench current leakage monitor for 4-Mb SPT CMOS DRAM technology. *Voldman, Steven H., +, T-SEM Aug 91 226-232*

**Integrated-circuit measurements; cf.** Current measurement; Integrated-circuit testing

#### Integrated-circuit metallization

electromigration ground rule generation utilizing Monte Carlo simulation methods. *Beitman, Bruce A., +, T-SEM Feb 91 63-66*

selective electroless plating for GaAs MMIC transmission line fabrication. *Choudhury, Debabani, +, T-SEM Feb 91 69-72*

**Integrated-circuit metallization; cf.** Integrated-circuit interconnections

**Integrated-circuit radiation effects; cf.** Integrated-circuit fabrication

#### Integrated-circuit reliability

evaluating VLSI reliability using hot carrier luminescence. *Uraoka, Yukiharu, +, T-SEM Aug 91 183-192*

latchup characterization using novel test structures and instruments for CMOS processes. *Cané, Carles, +, T-SEM Aug 91 199-205*

realistic statistical worst-case simulations of VLSI circuits using gradient analysis. *Bolt, Michael, +, T-SEM Aug 91 193-198*

**Integrated-circuit reliability; cf.** Electrostatic discharges

#### Integrated-circuit testing

chip test structure for the measurement of electrostatic discharge pulses. *Lendenmann, Heinz, +, T-SEM Aug 91 213-218*

design and use of microelectric test structures for characterization and control of IC manufacturing process (special issue). *T-SEM Aug 91 173-262*

multiplexed interconnect scheme for reducing number of contact pads on process control chips. *Walton, Anthony J., +, T-SEM Aug 91 233-240*

production scheduling algorithms for semiconductor test facility. *Uzsoy, Reha, +, T-SEM Nov 91 270-280*

using spatial information to analyze correlations between chip test structure data. *Kibarian, John K., +, T-SEM Aug 91 219-225*

**Integrated-circuit testing; cf.** Force measurement; Integrated-circuit reliability

**Integrated circuits; cf.** CMOS integrated circuits; Large-scale integration; MMICs; MOS integrated circuits; Ultra-large-scale integration; Very-large-scale integration

**Interconnections, integrated circuits; cf.** Integrated-circuit interconnections

**Ion ...; cf.** Plasma ...

**Ion implantation; cf.** Integrated-circuit ion implantation

## J

**JFET integrated circuits; cf.** JFETs

#### JFETs

characterization of parasitic bipolar and MOS transistors to evaluate CMOS process uniformity. *Wilson, David, +, T-SEM Aug 91 241-249*

**Junction FETs; cf.** JFETs

## K

**Knowledge-based systems; cf.** Expert systems

## L

**Lamps; cf.** Lighting

#### Large-scale integration

radiation thermometry of silicon wafers in diffusion furnace for fabrication of LSI circuits. *Watanabe, Tomoji, +, T-SEM Feb 91 59-63*

**Large-scale integration; cf.** Very-large-scale integration; Ultra-large-scale integration

**Latchup; cf.** Integrated-circuit reliability

**Learning systems; cf.** Neural networks

**Length; cf.** Size measurement

**Levitation; cf.** Magnetic levitation

#### Lighting

model for rapid thermal processing; achieving temperature uniformity through lamp control. *Gyurcsik, Ronald S., +, T-SEM Feb 91 9-13*

**Liquids; cf.** Water

**Lithography; cf.** Integrated-circuit fabrication

**Logic circuits; cf.** CMOS integrated circuits; MOS integrated circuits

**LSI; cf.** Large-scale integration

**Luminescent materials/devices**

evaluating VLSI reliability using hot carrier luminescence. *Uraoka, Yukiharu, +, T-SEM Aug 91 183-192*

## M

**Machining; cf.** Materials processing

**Magnetic bearings; cf.** Magnetic levitation

**Magnetic forces; cf.** Magnetic levitation

#### Magnetic levitation

magnetic levitation transport path. *Wang, Ing-Yann Albert, +, T-SEM Feb 91 145-154*

**Maintenance; cf.** Fault diagnosis

**Manufacturing; cf.** Integrated-circuit fabrication; Materials processing; Semiconductor device fabrication

#### Manufacturing automation

dynamic batching heuristic for simultaneous processing; using forecasting to reduce wait time in CIM environment. *Glassey, C. R., +, T-SEM May 91 77-82*

magnetic levitation transport path. *Wang, Ing-Yann Albert, +, T-SEM Feb 91 145-154*

**Manufacturing automation; cf.** Process control; Process monitoring

#### Manufacturing scheduling

production scheduling algorithms for semiconductor test facility. *Uzsoy, Reha, +, T-SEM Nov 91 270-280*

#### Materials processing

hybrid wafer-dicing process for GaAs MMIC production using spin-on wax. *Chang, Edward Y., +, T-SEM Feb 91 66-68*

**Materials processing; cf.** Integrated-circuit fabrication; Plasma applications, materials processing; Process control; Process heating

**Measurement; cf.** Capacitance measurement; Current measurement; Force measurement; Integrated-circuit measurements; Size measurement; Voltage measurement

**Mechanical factors; cf.** Contacts, mechanical factors

**Mechanical variables control; cf.** Fluid flow control

**Mechanical variables measurement; cf.** Force measurement; Measurement

**Memories; cf.** Random-access memories

**Metallization; cf.** Integrated-circuit metallization

#### Microscopy

modeling optical microscopes for wafer alignment and line-width measurement. *Yuan, Chi-Min, +, T-SEM May 91 99-110*

**Microwave integrated circuits; cf.** MMICs; Strip transmission lines

**Millimeter-wave integrated circuits; cf.** MMICs

**MISFETs; cf.** MOSFETs

#### MMICs

hybrid wafer-dicing process for GaAs MMIC production using spin-on wax. *Chang, Edward Y., +, T-SEM Feb 91 66-68*

methodology for guiding process-driven manufacturing organization instituting process control on facilitywide basis. *Moran, Peter W., +, T-SEM Nov 91 304-311*

selective electroless plating for GaAs MMIC transmission line fabrication. *Choudhury, Debabani, +, T-SEM Feb 91 69-72*

**Modeling; cf.** Optical components; Probes; Process heating; Semiconductor device fabrication; Statistics; Yield optimization

**Monitoring; cf.** Process monitoring

#### Monte Carlo methods

electromigration ground rule generation utilizing Monte Carlo simulation methods. *Beitman, Bruce A., +, T-SEM Feb 91 63-66*

#### MOS integrated circuits

self-multiplexing force-sense test structures for MOS IC application. *der Kluuw, Cornelis L. M., +, T-SEM Aug 91 206-212*

**MOS integrated circuits; cf.** CMOS integrated circuits; MOSFETs

**MOS integrated circuits, memory; cf.** CMOS integrated circuits, memory

**MOSFET circuits; cf.** MOS integrated circuits

**MOSFET switches; cf.** CMOSFET switches

#### MOSFETs

analysis of methods for determining dimensional offset of conductive layers and MOS transistors. *Swaving, Sieger, +, T-SEM Aug 91 17-21*



**FETs; cf.** MOS integrated circuits

## plexing

ultiplexed interconnect scheme for reducing number of contact pads on process control chips. *Walton, Anthony J.*, + , *T-SEM Aug 91* 233-240  
If-multiplexing force-sense test structures for MOS IC applications. *van der Klauw, Cornelis L. M.*, + , *T-SEM Aug 91* 206-212

## N

### al networks

ing influence diagrams and neural networks in modeling semiconductor manufacturing processes; adaptive learning architecture for LPCVD. *Nadi, Fariborz*, + , *T-SEM Feb 91* 52-58  
erical methods; **cf.** Monte Carlo methods

## O

### al components

odeling optical equipment for wafer alignment and line-width measurement. *Yuan, Chi-Min*, + , *T-SEM May 91* 99-110

### al position measurement

odeling optical equipment for wafer alignment and line-width measurement. *Yuan, Chi-Min*, + , *T-SEM May 91* 99-110

### al propagation; **cf.** Ultraviolet propagation

### al radiation effects; **cf.** Ultraviolet radiation effects

### ization methods; **cf.** Gradient methods

### ic materials/devices; **cf.** Carbon materials/devices

## P

### n clustering methods

stered defects in IC fabrication; impact on process control charts. *Friedman, David J.*, + , *T-SEM Feb 91* 36-42

### n recognition

erpretation and control of C-V measurements using pattern recognition and expert system techniques; C-V EXPERT. *Walls, Jim A.*, + , *T-SEM Aug 91* 250-262

### es; **cf.** Ultraviolet propagation

### r waveguides; **cf.** Strip transmission lines

### a applications, materials processing

-damage, low-contaminant ion plasma processing system for ULSI circuit manufacture using energy clean technology. *Goto, Haruhiro H.*, + , *T-SEM May 91* 111-121

istical experimental design in CCl<sub>4</sub>-plasma-etch modeling. *May, Gary*, + , *T-SEM May 91* 83-98

### a etching; **cf.** Plasma applications, materials processing

### on measurement; **cf.** Optical position measurement

### tion methods; **cf.** Forecasting

### bility

ct solution to Murphy's yield integral for compounding statistical distributions. *Stapper, C. H.*, *T-SEM Nov 91* 294-297

### s control

acterization of parasitic bipolar and MOS transistors to evaluate MOS process uniformity. *Wilson, David*, + , *T-SEM Aug 91* 241-249  
gn and use of microelectric test structures for characterization and nrol of IC manufacturing process (special issue). *T-SEM Aug 91* 3-262

hodology for guiding process-driven manufacturing organizations in stituting process control on facilitywide basis. *Moran, Peter W.*, + , *SEM Nov 91* 304-311

el for rapid thermal processing; achieving temperature uniformity ough lamp control. *Gyurcsik, Ronald S.*, + , *T-SEM Feb 91* 9-13

ultiplexed interconnect scheme for reducing number of contact pads on ocess control chips. *Walton, Anthony J.*, + , *T-SEM Aug 91* 233-240

inciples of wet chemical processing in ULSI microfabrication using vanced surface-active buffered hydrogen fluoride. *Kikuyama, rohisa*, + , *T-SEM Feb 91* 26-35

ess control system for VLSI fabrication. *Sachs, Emanuel*, + , *T-SEM ry 91* 134-144

**control; cf.** Manufacturing automation; Process heating; Process monitoring; Yield optimization

### heating

ess rapid thermal annealing of GaAs using graphite susceptor. *Kazior, omas E.*, + , *T-SEM Feb 91* 21-25

ufacturability issues in rapid thermal chemical vapor deposition. *türk, Mehmet C.*, + , *T-SEM May 91* 155-165

ufacturability issues related to transient thermal annealing of sputtered nium silicide films in rapid thermal processor. *Shenai, Krishna*, *SEM Feb 91* 1-8

el for rapid thermal processing; achieving temperature uniformity ough lamp control. *Gyurcsik, Ronald S.*, + , *T-SEM Feb 91* 9-13

author entry for coauthors

steady-state thermal uniformity and gas flow patterns in rapid thermal processing chamber; numerical calculations for various process conditions. *Campbell, Stephen A.*, + , *T-SEM Feb 91* 14-20

### Process heating; **cf.** Temperature measurement

### Process monitoring

continuous semiconductor manufacturing equipment diagnosis using evidence integration; LPCVD application. *Chang, Norman H.*, + , *T-SEM Feb 91* 43-51

### Production systems; **cf.** Process control

## R

### Radiation effects; **cf.** Ultraviolet radiation effects

### RAM; **cf.** Random-access memories

### Random-access memories

trench current leakage monitor for 4-Mb SPT CMOS DRAM technology. *Voldman, Steven H.*, + , *T-SEM Aug 91* 226-232

### Reliability; **cf.** Integrated-circuit reliability

### Reliability testing; **cf.** Integrated-circuit reliability

### Resistance

effects of backend processing on counterdoped N<sup>+</sup> poly-Si resistance. *Manos, Pete*, + , *T-SEM Nov 91* 288-293

### RTA (rapid thermal annealing); **cf.** Process heating

## S

### Scheduling; **cf.** Manufacturing scheduling

### Semiconductor charge carriers; **cf.** Charge-carrier processes

### Semiconductor device fabrication

using influence diagrams and neural networks in modeling semiconductor manufacturing processes; adaptive learning architecture for LPCVD. *Nadi, Fariborz*, + , *T-SEM Feb 91* 52-58

### Semiconductor device fabrication; **cf.** Integrated-circuit fabrication; Plasma applications, materials processing; Process heating

### Semiconductor device ion implantation; **cf.** Integrated-circuit ion implantation; Plasma applications, materials processing

### Semiconductor device measurements; **cf.** Integrated-circuit measurements

### Semiconductor device metallization; **cf.** Integrated-circuit metallization

### Semiconductor device reliability; **cf.** Electrostatic discharges; Integrated-circuit reliability

### Semiconductor device testing; **cf.** Integrated-circuit testing

### Semiconductor devices; **cf.** MOSFETs

### Semiconductor memories; **cf.** CMOS integrated circuits, memory

### Semiconductor switches; **cf.** CMOSFET switches

### Silicon materials/devices

effects of backend processing on counterdoped N<sup>+</sup> poly-Si resistance. *Manos, Pete*, + , *T-SEM Nov 91* 288-293

### Silicon materials/devices; **cf.** Titanium materials/devices

### Simulation; **cf.** Monte Carlo methods; Statistics

### Size measurement

analysis of methods for determining dimensional offset of conducting layers and MOS transistors. *Swaving, Sieger*, + , *T-SEM Aug 91* 174-182

modeling optical equipment for wafer alignment and line-width measurement. *Yuan, Chi-Min*, + , *T-SEM May 91* 99-110

### Special issues/sections

design and use of microelectric test structures for characterization and control of IC manufacturing process. *T-SEM Aug 91* 173-262

### Statistics

realistic statistical worst-case simulations of VLSI circuits using gradient analysis. *Bolt, Michael*, + , *T-SEM Aug 91* 193-198

statistical experimental design in CCl<sub>4</sub>-plasma-etch modeling. *May, Gary S.*, + , *T-SEM May 91* 83-98

### Statistics; **cf.** Probability

### Strip transmission lines

selective electroless plating for GaAs MMIC transmission line fabrication. *Choudhury, Debabani*, + , *T-SEM Feb 91* 69-72

## T

### Temperature control

model for rapid thermal processing; achieving temperature uniformity through lamp control. *Gyurcsik, Ronald S.*, + , *T-SEM Feb 91* 9-13

### Temperature control; **cf.** Process heating

### Temperature measurement

radiation thermometry of silicon wafers in diffusion furnace for fabrication of LSI circuits. *Watanabe, Tomoji*, + , *T-SEM Feb 91* 59-63

† Check author entry for subsequent corrections/comments



**Testing; cf.** Fault diagnosis; Integrated-circuit testing  
**Thermal factors; cf.** Process heating; Semiconductor device fabrication  
**Thermal variables control; cf.** Process heating; Temperature control  
**Thermal variables measurement; cf.** Temperature measurement

#### Thin-film circuit fabrication

manufacturability issues related to transient thermal annealing of sputtered titanium silicide films in rapid thermal processor. *Shenai, Krishna, T-SEM Feb 91 1-8*

#### Titanium materials/devices

manufacturability issues related to transient thermal annealing of sputtered titanium silicide films in rapid thermal processor. *Shenai, Krishna, T-SEM Feb 91 1-8*

using screening and response-surface experimental designs to develop 0.5- $\mu$ m CMOS self-aligned titanium silicide process. *Jones, Robert E., +, T-SEM Nov 91 281-287*

**Tolerance analysis/assignment; cf.** Yield optimization

**Transistors; cf.** JFETs; MOSFETs

**Transmission lines; cf.** Strip transmission lines

**Transmission measurements; cf.** Ultraviolet propagation

## U

#### Ultra-large-scale integration

low-damage, low-contaminant ion plasma processing system for ULSI circuit manufacture using energy clean technology. *Goto, Haruhiro H., +, T-SEM May 91 111-121*

principles of wet chemical processing in ULSI microfabrication using advanced surface-active buffered hydrogen fluoride. *Kikyuama, Hirohisa, +, T-SEM Feb 91 26-35*

#### Ultraviolet propagation

transmission measurements of pellicles for deep-UV lithography. *Partlo, William N., +, T-SEM May 91 128-133*

#### Ultraviolet radiation effects

removing organic impurities in ultrapure water systems; effect of component interactions with UV radiation. *Governal, Robert, +, T-SEM Nov 91 298-303*

**Ultraviolet radiation effects; cf.** Integrated-circuit fabrication

## V

#### Very-large-scale integration

analysis of methods for determining dimensional offset of conductive layers and MOS transistors. *Swaving, Sieger, +, T-SEM Aug 91 171-175*  
 defect size distribution in VLSI chips; analytical model for short circuit related to line spacing. *Glang, Reinhard, T-SEM Nov 91 265-269*  
 evaluating VLSI reliability using hot carrier luminescence. *Uyama, Yukiharu, +, T-SEM Aug 91 183-192*

process control system for VLSI fabrication. *Sachs, Emanuel, +, T-SEM May 91 134-144*

realistic statistical worst-case simulations of VLSI circuits using genetic algorithms. *Bolt, Michael, +, T-SEM Aug 91 193-198*

**VLSI; cf.** Very-large-scale integration

#### Voltage measurement

interpretation and control of C-V measurements using pattern recognition and expert system techniques; C-V EXPERT. *Walls, Jim A., +, T-SEM Aug 91 250-262*

## W

#### Water

removing organic impurities in ultrapure water systems; effect of component interactions with UV radiation. *Governal, Robert, +, T-SEM Nov 91 298-303*

**Wiring; cf.** Integrated-circuit interconnections

## Y

#### Yield optimization

clustered defects in IC fabrication; impact on process control. *Friedman, David J., +, T-SEM Feb 91 36-42*

defect size distribution in VLSI chips; analytical model for short circuit related to line spacing. *Glang, Reinhard, T-SEM Nov 91 265-269*  
 exact solution to Murphy's yield integral for compounding statistical distributions. *Stapper, C. H., T-SEM Nov 91 294-297*

manufacturability issues related to transient thermal annealing of sputtered titanium silicide films in rapid thermal processor. *Shenai, Krishna, T-SEM Feb 91 1-8*



IF YOU WERE UNABLE TO ATTEND  
A RECENT CONFERENCE



YOU CAN STILL ORDER THE CONFERENCE PROCEEDINGS

TO ORDER OR TO REQUEST A FREE CATALOG

TOLL-FREE IN THE U.S. AND CANADA CALL  
**1-800-678-IEEE**

IN OTHER COUNTRIES CALL  
**(908) 981-0060**

**FAX (908) 981-9667**

OR WRITE  
IEEE CUSTOMER SERVICE DEPARTMENT  
445 HOES LANE, PO BOX 1331  
PISCATAWAY, NJ 08855-1331 U.S.A.

IN EUROPE, THE MIDDLE EAST, AFRICA OR THE USSR  
CONTACT THE NEW BRUSSELS OFFICE

**CALL 32.2.770.22.42.**

**FAX 32.2.770.85.05**

OR WRITE  
IEEE TAB OFFICE  
13, AVENUE DE L'AQUILON  
B-1200 BRUSSELS BELGIUM



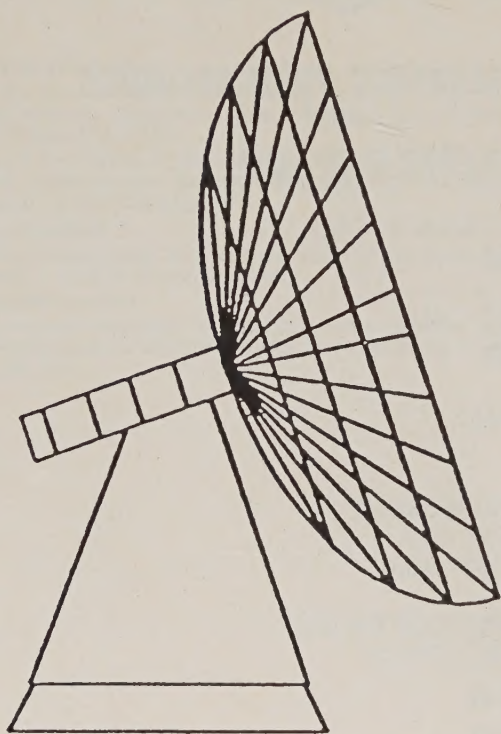
**IEEE**

A SERVICE OF IEEE TECHNICAL ACTIVITIES DEPARTMENT

# Satellite Communications

Combines a solid review of fundamentals with the practical knowledge that an engineer needs to stay ahead in this fast-growing field and provides examples of real-world systems and their problems, as well as an explanation of the technical history behind today's systems.

An exploration of the complete system--from spacecraft to discussion of the atmosphere through which signals pass.



The program's study guide is of great value to the working engineer who is familiar with communication theory but who needs to know more about its application to the satellite channel. It will also assist the engineer who needs to relate package design to the overall spacecraft.

Program includes a study guide with solutions manual, final exam, and textbook, *Satellite Communications*, by Timothy Pratt and Charles Bostian, John Wiley and Sons, 1986.

Satellite Communications is **IEEE member priced at \$199** (\$398 non-member). Plus shipping and handling. For a full description of the program and complete ordering information, call IEEE today at **1-800-678-IEEE....Telex: 833233....Fax: 1-201-981-1686.**

Or write to: **IEEE**  
Educational Activities Department  
445 Hoes Lane  
PO Box 1331  
Piscataway, NJ 08855-1331





## INFORMATION FOR AUTHORS

### Content

IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING is published quarterly with the first issue in February. Contributed papers may be of a tutorial or research nature, but the latter must be original and must not duplicate descriptions or derivations available elsewhere.

This TRANSACTIONS aims to address the challenging problems of manufacturing complex microelectronic components, especially very large scale integrated circuits (VLSI), but also thin-film heads for magnetic recording, integrated optical components, and other similar products. Manufacturing these products typically requires precision micropatterning, precision control of materials properties, ultra-clean work environments, and complex interactions of chemical, physical, electrical, and mechanical processes. An integrated application of interdisciplinary skills is essential for success.

Particularly sought for these TRANSACTIONS are original papers describing practical engineering techniques for solving problems involving interactions among facility, equipment, process, product, and people issues in the context of manufacturing. The TRANSACTIONS' spectrum of coverage will range from fundamental to applied. Whenever possible papers should include appropriate results from manufacturing experience.

Submission of a manuscript manifests the fact that it has been neither copyrighted, published, nor submitted or accepted for publication elsewhere, unless otherwise so stated by the author.

### Length

Authors should document their work in relation to the open literature. The following limits on length will be enforced.

- 1) Regular papers, 7 to 20 double-spaced pages in length, plus up to 10 pages, 8½" by 11" of figures.
- 2) Correspondence items of less than 6 double-spaced pages, plus not more than 3 pages of figures.

### Style for Manuscripts

1) The manuscript should be printed using double space; use one side of the sheet only. Office-duplicated copies are acceptable.

2) Provide a carefully worded abstract of from 100 to 200 words for papers and less than 50 words for correspondence. Name, address, and telephone number of author(s) should appear with abstract.

3) A pamphlet, "Information for IEEE Transactions and Journal Authors," is available on request from the IEEE Publications Department, 345 East 47 Street, New York, NY 10017.

4) References may appear as numbered footnotes or in a separate bibliography at the end of the paper. In either case, references should be complete and in IEEE style.

*Style for papers:* Author (with initials first), title, journal title, volume number, inclusive page numbers, month, year.

*Style for books:* Author, title, location publisher, year, page or chapter number (if desired). See this issue for further examples.

5) Figure captions should be on a separate sheet in proper style for typesetting. See this issue for examples.

6) Departures from the above style may delay publication.

### Style for Illustrations

1) Originals of drawings and glossy print photographs should be sharp and of good contrast. Line drawings should be in high contrast black ink on a white background. Use 8½" × 11" size sheets to simplify handling of the manuscript. Template lettering is recommended; typing on figures is not acceptable. Lettering must be large enough to permit legible reduction of the figure to column width, perhaps as much as 4:1.

2) Identify each illustration on the back or at the bottom of the front with the figure number and name of author(s). *Captions lettered on figures will be blocked out in reproduction in favor of typeset captions.*

### Review Process

The review process usually requires about two months. The author is then notified of the decision of the Editor or Associate Editor based on reviewer recommendations. The authors may be asked to modify the manuscript if it is not accepted or rejected in its original form. The elapsed time between final acceptance of a manuscript and publication is usually four to eight months.

### Submissions

Send the original and three copies of your manuscript to the Editor. Each copy should be complete with illustrations and should be accompanied by a separate sheet containing the address to which galley proofs and other correspondence can be sent. Also enclose original illustrations or be prepared to submit these immediately upon acceptance of your manuscript. Authors will be charged for changes in text or figures in proof. In the case of regular papers, also be prepared to provide a brief technical biography and photograph of each author.

**Voluntary Page Charges:** After a manuscript has been accepted for publication, the author's company or institution will be requested to pay a voluntary charge of \$110.00 per printed page to cover part of the cost of publication. Page charges for this IEEE TRANSACTIONS, like those for journals of other professional societies, are not obligatory nor is their payment a prerequisite for publication. The author will receive 100 free reprints without covers if the charge is honored. Detailed instructions will accompany the galley proof.

**Copyright:** It is the policy of the IEEE to own the copyright to the technical contributions it publishes on behalf of the interests of the IEEE, its authors, and their employers, and to facilitate the appropriate reuse of this material by others. To comply with the U.S. Copyright Law, authors are required to sign an IEEE copyright transfer form before publication. This form, a copy of which appears in the February 1991 issue of this TRANSACTIONS, returns to authors and their employers full rights to reuse their material for their own purposes. Authors must submit a signed copy of this form with their manuscripts.



